What is claimed is:

1. An apparatus, for use in a semiconductor device, for providing a domain crossing operation, comprising:

a domain crossing sensing block in response to an operation mode signal, first and second delay locked loop (DLL) clock signals and a CAS latency, generating a plurality of selection signals;

an output enable signal generator in response to the plurality of selection signals, generating a plurality of output enable signals;

a data control block in response to the output enable signals and the CAS latency, controlling a data output operation of the semiconductor device; and

a plurality of data align blocks, each in response to the selection signals, the first and second DLL clock signals and an address signal, aligning data corresponding to the address signal in the data output operation.

2. The apparatus as recited in claim 1, wherein the operation mode signal includes a refresh state signal, a DLL disable signal and a RAS idle signal.

3. The apparatus as recited in claim 1, wherein the output enable signal generator includes:

a first output enable signal generator for generating an initialization signal synchronized with an internal clock in response to a read instruction; and

a second output enable signal generator for generating the enable signals by delaying the initialization signal based on the selection signals.

4. The apparatus as recited in claim 3, wherein the second output enable signal generator includes:

a selection block for receiving the initialization signal and selecting one of first and second initialization signals synchronized with the first and second DLL clock signals in response to the selection signal;

a first generating block in response to the first DLL clock signal for generating some of the enable signals based on the selected initialization signal; and

a second generating block in response to the second DLL clock signal for generating the other of the enable signals based on the selected initialization signal.

5. The apparatus as recited in claim 4, wherein the selection block includes a MUX.

6. The apparatus as recited in claim 5, wherein the selection block includes a flip-flop for receiving an output signal from the MUX at an input terminal, the first DLL clock signal at a clock terminal and the selection signal at a reset terminal and synchronizing the output signal from the first MUX with the first DLL clock signal.

7. The apparatus as recited in claim 4, wherein the first generating block includes:

a first flip-flop group for receiving an output signal from the selection block, wherein the first flip-flop group has a plurality of flip-flops which receive respectively the first DLL clock signal at a clock terminal, the selection signal at a reset terminal and an output signal of the last flip-flop at an input terminal and generate individually first control signals synchronized with the first DLL clock signal;

a MUX for selecting one of the first control signals in response to the selection signals; and

a second flip-flop group for receiving an output signal from the MUX and generating the enable signals.

8. The apparatus as recited in claim 4, wherein the second generating block includes:

a first flip-flop group for receiving an output signal from the selection block, wherein the first flip-flop group has a plurality of flip-flops which receive respectively the second DLL clock signal at a clock terminal, the selection signal at a reset terminal and an output signal of the last flip-flop at an input terminal and generate individually second control signals synchronized with the second DLL clock signal;

a MUX for selecting one of the second control signals in response to the selection signals; and

a second flip-flop group for receiving an output signal from the MUX and generating the enable signals.

9. The apparatus as recited in claim 2, wherein the domain crossing sensing block includes:

a sensing control signal generator for generating a sensing start signal in response to the refresh state signal, the DLL disable signal and the RAS idle signal;

a phase detector for comparing the first DLL clock signal with the second DLL clock signal in response to the sensing start signal and generating one of the selection signals, which is activated during the CAS latency, and a phase detection signal, which defines a phase detection period, in response to the sensing start signal;

a reading path modeling block for delaying the phase

detection signal by a predetermined value, which is equal to a delay time occurred through data reading path, and generating a delayed phase detection signal; and

a latency detector for comparing the delayed phase detection signal with the CAS latency synchronized with the internal clock and generating others of the selection signals.

10. The apparatus as recited in claim 9, wherein the phase detector includes:

a first MUX for selecting one of the first and second DLL clock signals in response to the setup selection signal; and

a flip-flop for receiving an output signal from the first MUX at an input terminal, the first DLL clock signal at a clock terminal and the sensing start signal at a reset terminal.

11. The apparatus as recited in claim 9, wherein the latency detector includes:

a flip-flop block having a plurality of flip-flops, each receiving the internal clock at a clock terminal, the sensing start signal at a reset terminal and a supply voltage at an input terminal, for generating first and second delay sensing signals;

a delay block for delaying the sensing start signal;

a flight timing sensing block for generating a plurality of flight detection signals in response to the first and second delay sensing signals; and

a selector for outputting the plurality of output enable signals in response to the plurality of flight detection signals.

12. The apparatus as recited in claim 1, wherein the data control block includes:

a data controller for receiving the enable signals and generating a data enable signal defining a valid period of an outputted data; and

a data output controller for receiving the output enable signals and generating a data strobe enable signal defining an active period of a data strobe signal.

13. The apparatus as recited in claim 12, wherein the data output controller includes:

a plurality of enable signal generators for respectively receiving the enable signals and individually generating the data strobe enable signal by transmitting one of the enable signals in response to a modified CAS latency,

wherein the modified CAS latency is generated by a NOR operation on at least two CAS latencies.

14. The apparatus as recited in claim 12, wherein the data controller includes:

a plurality of control signal generators for respectively receiving the enable signals and individually generating the data enable signal by transmitting one of the enable signals in response to a modified CAS latency,

wherein the modified CAS latency is generated by a NOR operation on at least two CAS latencies.

15. The apparatus as recited in claim 1, wherein the align block includes:

a first generating block in response to the first and second DLL clock signal generating a plurality of align initial signals based on the address signal; and

a second generating block in response to the selection signal generating a data align signal based on the align initial signals.

16. The apparatus as recited in claim 15, wherein the first generating block includes:

a MUX for selecting one of the first and second DLL clock signals in response to the selection signal;

a first flip-flop for receiving an output signal from the MUX at an input terminal and the first DLL clock signal at a clock terminal and synchronizing the output signal from the MUX with the first DLL clock signal to output one of the align initial signal; and

a second flip-flop group for receiving the output signal from the first flip-flop, wherein the second flip-flop group has a plurality of flip-flops which receive respectively the second DLL clock signal at a clock terminal and an output signal of the last flip-flop at an input terminal and individually generate the other of the align initial signals synchronized with the second DLL clock signal.

17. The apparatus as recited in claim 15, wherein the second generating block includes:

a MUX for selecting one among the align initial signals in response to the selection signals;

a flip-flop group for receiving an output signal from the MUX, wherein the flip-flop group has a plurality of flip-flops which receive respectively the second DLL clock signal at a clock terminal and an output signal of the last flip-flop at an input terminal and generate individually align control signals synchronized with the second DLL clock signal; and

a signal generator for receiving the output signal from

the MUX and the align control signals and outputting the data align signal in response to the CAS latency.

18. A semiconductor device for providing a domain crossing operation, comprising:

a domain crossing sensing block in response to a operation mode signal, first and second delay locked loop (DLL) clock signals and a CAS latency generating a plurality of selection signals;

an output enable signal generator in response to the plurality of selection signals generating a plurality of output enable signals;

a data control block in response to the output enable signals and the CAS latency controlling a data output operation in the semiconductor device; and

a plurality of data align block, each in response to the selection signals, the first and second DLL clock signals and an address signal aligning data corresponding to the address signal in the data output operation.

19. The semiconductor device as recited in claim 18, wherein the operation mode signal includes a refresh state signal, a DLL disable signal and a RAS idle signal.

20. The semiconductor device as recited in claim 18, wherein the output enable signal generator includes:

a first output enable signal generator for generating an initialization signal synchronized with an internal clock in response to a read instruction; and

a second output enable signal generator for generating the enable signals by delaying the initialization signal based on the selection signals.

21. The semiconductor device as recited in claim 20, wherein the second output enable signal generator includes:

a selection block for receiving the initialization signal and selecting one of first and second initialization signals synchronized with the first and second DLL clock signals in response to the selection signal;

a first generating block in response to the first DLL clock signal generating some of the enable signals based on the selected initialization signal; and

a second generating block in response to the second DLL clock signal generating the other of the enable signals based on the selected initialization signal.

22. The semiconductor device as recited in claim 21, wherein the selection block includes a MUX.

23. The semiconductor device as recited in claim 22, wherein the selection block includes a flip-flop for receiving an output signal from the MUX at an input terminal, the first DLL clock signal at a clock terminal and the selection signal at a reset terminal and synchronizing the output signal from the first MUX with the first DLL clock signal.

24. The semiconductor device as recited in claim 21, wherein the first generating block includes:

a first flip-flop group for receiving an output signal from the selection block, wherein the first flip-flop group has a plurality of flip-flops which receive respectively the first DLL clock signal at a clock terminal, the selection signal at a reset terminal and an output signal of the last flip-flop at an input terminal and generate individually first

control signals synchronized with the first DLL clock signal;

a MUX for selecting one of the first control signals in response to the selection signals; and

a second flip-flop group for receiving an output signal from the MUX and generating the enable signals.

25. The semiconductor device as recited in claim 21, wherein the second generating block includes:

a first flip-flop group for receiving an output signal from the selection block, wherein the first flip-flop group has a plurality of flip-flops which receive respectively the second DLL clock signal at a clock terminal, the selection signal at a reset terminal and an output signal of the last flip-flop at an input terminal and generate individually second control signals synchronized with the second DLL clock signal;

a MUX for selecting one of the second control signals in response to the selection signals; and

a second flip-flop group for receiving an output signal from the MUX and generating the enable signals.

26. The semiconductor device as recited in claim 19, wherein the domain crossing sensing block includes:

a sensing control signal generator for generating a sensing start signal in response to the refresh state signal, the DLL disable signal and the RAS idle signal;

a phase detector for comparing the first DLL clock signal with the second DLL clock signal in response to the sensing start signal and generating one of the selection signals, which is activated during the CAS latency, and a phase detection signal, which defines a phase detection period, in response to the sensing start signal;

a reading path modeling block for delaying the phase detection signal by a predetermined value, which is equal to a delay time occurred through data reading path, and generating a delayed phase detection signal; and

a latency detector for comparing the delayed phase detection signal with the CAS latency synchronized with the internal clock and generating others of the selection signals.

27. The semiconductor device as recited in claim 26, wherein the phase detector includes:

a first MUX for selecting one of the first and second DLL clock signals in response to the setup selection signal; and

a flip-flop for receiving an output signal from the first MUX at an input terminal, the first DLL clock signal at a clock terminal and the sensing start signal at a reset terminal.

28. The semiconductor device as recited in claim 26, wherein the latency detector includes:

a flip-flop block having a plurality of flip-flops, each receiving the internal clock at a clock terminal, the sensing start signal at a reset terminal. and a supply voltage at an input terminal, for generating first and second delay sensing signals;

a delay block for delaying the sensing start signal;

a flight timing sensing block for generating a plurality of flight detection signals in response to the first and second delay sensing signals; and

a selector for outputting the plurality of output enable signals in response to the plurality of flight detection signals.

29. The semiconductor device as recited in claim 18, wherein the data control block includes:

a data controller for receiving the enable signals and generating a data enable signal defining a valid period of an outputted data; and

a data output controller for receiving the output enable signals and generating a data strobe enable signal defining an active period of a data strobe signal.

30. The semiconductor device as recited in claim 29, wherein the data output controller includes:

a plurality of enable signal generators for respectively receiving the enable signals and individually generating the data strobe enable signal by transmitting one of the enable signals in response to a modified CAS latency,

wherein the modified CAS latency is generated by a NOR operation on at least two CAS latencies.

31. The semiconductor device as recited in claim 29, wherein the data controller includes:

a plurality of control signal generators for respectively receiving the enable signals and individually generating the data enable signal by transmitting one of the enable signals in response to a modified CAS latency,

wherein the modified CAS latency is generated by a NOR operation on at least two CAS latencies.

32. The semiconductor device as recited in claim 18, wherein the align block includes:

a first generating block in response to the first and second DLL clock signal generating a plurality of align

initial signals based on the address signal; and

a second generating block in response to the selection signal generating a data align signal based on the align initial signals.

33. The semiconductor device as recited in claim 32, wherein the first generating block includes:

a MUX for selecting one of the first and second DLL clock signals in response to the selection signal;

a first flip-flop for receiving an output signal from the MUX at an input terminal and the first DLL clock signal at a clock terminal and synchronizing the output signal from the MUX with the first DLL clock signal to output one of the align initial signal; and

a second flip-flop group for receiving the output signal from the first flip-flop, wherein the second flip-flop group has a plurality of flip-flops which receive respectively the second DLL clock signal at a clock terminal and an output signal of the last flip-flop at an input terminal and individually generate the other of the align initial signals synchronized with the second DLL clock signal.

34. The semiconductor device as recited in claim 32, wherein the second generating block includes:

a MUX for selecting one among the align initial signals in response to the selection signals;

a flip-flop group for receiving an output signal from the MUX, wherein the flip-flop group has a plurality of flip-flops which receive respectively the second DLL clock signal at a clock terminal and an output signal of the last flip-flop at an input terminal and generate individually align control signals synchronized with the second DLL clock signal; and

a signal generator for receiving the output signal from the MUX and the align control signals and outputting the data align signal in response to the CAS latency.